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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,977	09/22/2003	Koji Hosono	002372.00046	4948

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EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,977	HOSONO ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *12 and 14-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 9* is/are rejected.

7)☒ Claim(s) *2-8,10-11,13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/800913.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/03; 10/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicants' election without traverse of Group I, claims 1-11 and 13, in the reply filed on April 27, 2005 is acknowledged.

2. Claims 12, 14-32 are withdrawn from further consideration. Applicants are requested to cancel claims 12, 14-32 in the next response.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: DATA-REPROGRAMMING/RETRIEVAL CIRCUIT TEMPORARILY STORE PROGRAMMED/RETRIEVED DATA FOR CACHING AND MULTILEVEL LOGICAL FUNCTIONS IN AN EEPROM

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Takeuchi et al. (U.S. Patent No. 6,046,935).

Regarding claim 1, Takeuchi discloses a non-volatile semiconductor device comprising:

a memory cell array having electrically erasable programmable non-volatile memory cells (see FIG. 3);

a plurality of reprogramming and retrieval circuits (data circuits 6**-0 to 6**-m, see FIGS. 10 and 12) that temporarily store data to be programmed in the memory cell array and sense data retrieved from the memory cell array, each reprogramming and retrieval circuit (see FIG. 15 for details) having a first latch (FF1 comprising Qp9, Qp10, Qn21, Qn22, see Fig. 15) and a second latch (FF2 comprising Qp16, Qp17, Qn29, Qn30, see FIG. 15), the first latch being connected to a selected bit line (BLa, see FIG. 15) of the memory cell array via a first transfer switch (Qn39, see FIG. 15) and a second transfer switch (Qn24, see FIG. 15) series-connected to each other, the second latch being connected to a connection node of the first and the second transfer switches via a third transfer switch (Qn32, see FIG. 15), a data node of the second latch (outputs of FF2, see FIG. 15) being connected to data input and output lines (IOC and IOD, see FIG. 15) via column selection switches (Qn35 and Qn36, see FIG. 15); and

a controller (Control Gate/Select Gate Driving Circuit 21 for inherently generating signals BLCA, RV1A, RV2A controlling switches Qn39, Qn21, Qn32, see FIGS. 15 and 48) that controls the reprogramming and retrieval circuits on data-reprogramming operation to and data-retrieval operation from the memory cell array. (See column 27, line 11 to column 28, line 19)

Regarding claim 9, Takeuchi discloses wherein each reprogramming and retrieval circuit is selectively connected to a plurality of bit lines of the memory cell array via a bit line

selection switch (as shown in FIG. 15; each data circuit is connected to bit lines BLa and BLb via switches SG1A and SG1B).

Allowable Subject Matter

6. Claims 2-8, 10-11, 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed invention having the following limitations, in combination with the remaining claimed limitations:

i) wherein after the data has been programmed in a selected memory cell, the programmed data is retrieved for programming verification, the retrieved data being **sensed and stored** in the first latch (as in claim 2); or

ii) in the caching operation mode, data transfer between one of the memory cells selected in accordance with a first address and the first latch being performed while data transfer is being performed between the second latch and input/output terminals in accordance with a second address with respect to one-bit two-level data to be stored in one of the memory cells (as in claim 3); or

iii) wherein each reprogramming and retrieval circuit has a common signal line connected to the connection node of the first and the second transfer switches via a fourth transfer switch (as in claim 10); or

iv) in a test mode, a cell current flowing in the selected memory cell is retrieved to the input and output terminals while the data programming cycle is interrupted during which the data retrieved by the retrieval for programming verification is stored in the first latch and the second latch is inactive (as in claim 13).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 23, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824